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Raymond Sun
12420 Woodhall Way
Tustin, CA 92782

EXAMINER	
SCHELL, JOSEPH O	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,185	CHUANG ET AL.	
	Examiner	Art Unit	
	Joseph Schell	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-25* is/are allowed.

6)☒ Claim(s) *1-22 and 26-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1-32 have been examined.

Claims 1-22 and 26-32 have been rejected.

Miscellaneous Note: The last reference in the IDS submitted February 20, 2004 appears very unrelated to this case and may have been cited in error. A brief search of patents by Mann in November of 1999 did not return any apparently-related references.

Claim Objections

1. The way that claim 9 states that the emulator returns data and status "under one of two conditions" and then lists two conditions, especially with the use of "two conditions" stated within the preamble of the claim, leaves the claim indefinite as to whether the claim requires checking for both conditions or just either condition. Also, the two possibilities would more accurate be described as processes, methods or steps instead of conditions. Examiner is assuming just one condition needs to be checked. If this were accurate the claim would be clearer if it read "returns data and status to said debugger unit by way of:" or something similar.

2. Claim 26 line 13 and claim 32 line 9 should include an "and" at the end.

Allowable Subject Matter

3. Claims 23-25 are allowable.

Within claim 23, the examiner deems the novel subject matter to be, within the context of the claim as a whole, that the bus mapping unit is located within the same board as the target MCU and debugger RAM, separate from the emulator board.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 5, 14, 19, 23 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 5 and 14 use the terms "free-run," "step-into," step-out" and "stop" test steps. These terms are not defined within the specification or generally known within the art.

6. Claim 19 line 5, claim 23 line 5 and claim 26 line 11 state "a debugger MCU, **implemented with** said target MCU." This use of "implemented with" seemingly implies a relational limitation, while the broadest reasonable interpretation of the term's use is that both the debugger MCU and target MCU simply exist within the same system. This broadest reasonable interpretation is not further limiting than the term's omission from the claim. Its inclusion in the claim is therefore indefinite because it is seemingly unneeded.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being unpatentable over Boyce (US Patent 5,796,258).

8. As per claim 1, Boyce ('258) discloses an apparatus for debugging an electronic system, said electronic system including a target microcontroller (MCU) and at least one ROM connected together (column 2 lines 43-48), comprising:

a debugger unit which debugs said target MCU (column 1 lines 49-52);

a ROM/RAM emulator/debugger unit, connected to said target MCU and said debugger unit, for emulating said ROM (column 1 lines 49-52), and including:

a ROM/RAM emulation memory, connected to said emulator/debugger unit, for storing user program codes downloaded from said debugger unit (column 2 lines 67-68 and column 3 lines 15-20);

an emulator/debugger microcontroller (MCU), coupled to said emulator/debugger unit, for communicating with, and performing requests from, said debugger unit and said target MCU (column 1 lines 57-61 and 2 lines 43-48,

while a microcontroller is not explicitly stated, it is required to perform the stated functions);

a bus mapping unit, coupled to said emulator/debugger MCU (column 2 line 67 through column 3 line 2); and

a debugger RAM unit, coupled to said emulator/debugger MCU (as shown in Figure 3 part of the ROM emulator's memory is dedicated to monitor code, see also column 3 lines 10-12).

9. As per claim 2, Boyce ('258) discloses the apparatus of claim 1, further comprising a debugger service routine ("debugger SR") downloaded from said debugger unit into said ROM/RAM emulation memory with said user program codes from said debugger unit (column 1 lines 55-57).

10. As per claim 3, Boyce ('258) discloses the apparatus of claim 2, further comprising a communication buffer implemented in said emulation memory, said communication buffer being disposed to store status, request and data by said target MCU and by said emulator/debugger MCU (column 3 lines 49-54, execution results are returned to the debugger, and execution status is conveyed the execution results. Also see column 2 lines 45-47, command fragments of debug routines are passed through the communications buffer).

11. As per claim 4, Boyce ('258) discloses the apparatus of claim 3, wherein said target MCU executes said debugger SR to:

copy a "loop to itself" instruction to said debugger RAM unit and then jump to said copied instruction to release access of said ROM/RAM emulation memory (column 3 lines 13-15 and 20-25);

inform said debugger unit upon executing a software breakpoint or upon completing requests from said emulator/debugger MCU (column 3 lines 49-54, the results are shown on the host debugger's display); and

parse requests from said emulator/debugger MCU to perform actions, wherein said requests are stored in one of said emulator/debugger RAM unit and said communication buffer (column 2 lines 45-47).

12. As per claim 5, Boyce ('258) discloses the apparatus of claim 1, wherein said debugger unit is disposed to:

download and upload user program codes to and from the emulator/debugger MCU (column 3 lines 15-20);

set, delete, enable and disable breakpoints (column 3 lines 39-42);

writes codes to the ROM/RAM emulation memory (column 3 lines 39-42);

show and modify registers and memory (column 3 lines 39-42); and

perform free-run, step-into, step-out and stop test steps (column 3 lines 39-42, the removal or placement of breakpoints controls the flow of a test routine).

13. As per claim 6, Boyce ('258) discloses the apparatus of claim 5, wherein said debugger RAM unit is disposed to:

store data for said target MCU to modify its debugging state and data (column 3 lines 39-42, modification of breakpoints changes the debug state and data);

store a request for said target MCU (column 3 lines 48-49);

store debugging status and data of said target MCU for uploading to said debugger unit after said target MCU has finished said request (column 3 lines 49-54); and

provide program spaces for said target MCU to execute programs in order to release access to said ROM/RAM emulation memory (column 3 lines 13-15).

14. As per claim 7, Boyce ('258) discloses the apparatus of claim 1, wherein said bus mapping unit maps said debugger RAM unit to a specified address space, which is different from said ROM/RAM emulation memory, to form a continuous and linear addressing space (column 3 lines 10-13, and as shown by Figure 3 with the separate memory addresses for user code and monitor instructions).

15. As per claim 8, Boyce ('258) discloses the apparatus of claim 3, wherein said emulator/debugger MCU passes debugging requests to said target MCU by one of:

a) said emulator/debugger MCU storing requests in said debugger RAM unit (column 1 lines 49-57);

said emulator/debugger MCU informing said target MCU to perform said requests (column 1 lines 54-56, the user initiates an interrupt);

said target MCU executing programs in said ROM/RAM emulation memory (column 1 lines 56-57); and

b) said emulator/debugger MCU informing said target MCU to perform said requests (column 1 lines 54-56);

said emulator/debugger MCU informing said target MCU to copy a "loop to itself" instruction to said debugger RAM unit (column 3 lines 20-22) ;

said target MCU jumping to said copied instruction to release access to said ROM/RAM emulation memory (column 3 lines 33-41); and

upon release by said target MCU, said emulator/debugger MCU storing requests in said communication buffer and informing said target MCU to perform said requests (column 3 lines 39-49).

16. As per claim 9, Boyce ('258) discloses the apparatus of claim 8, wherein said emulator/debugger MCU returns data and status to said debugger unit under one of two conditions:

a) after said target MCU has executed a software breakpoint instruction, after being informed by said target MCU, said emulator/debugger MCU uploads the content of one of said debugger RAM unit or communication buffer to said debugger unit (column 3 lines 32-49 and column 3 lines 55-57); or

b) after said target MCU has finished a request by said debugger unit, after being informed by said target MCU, said emulator/debugger MCU uploads the content of one of said debugger RAM unit and communication buffer to said debugger unit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 10-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyce ('258) in view of Autrey (US Patent 5,774,695).

18. As per claim 10, Boyce ('258) discloses an apparatus for debugging an electronic system, comprising:

a target board that includes a target MCU that has a ROM (column 2 lines 21-24);

a debugger unit for debugging said target MCU (column 2 lines 43-48, the mainframe); and

a ROM/RAM emulator board, connected to said debugger unit, for emulating said ROM of said target MCU, said emulator board including a ROM/RAM emulation

memory and an emulator MCU, said ROM/RAM emulation memory being disposed to store user program codes downloaded from said debugger unit, and said emulator MCU being disposed to read and write data from and to said ROM/RAM emulation memory.

Boyce ('258) anticipates a system wherein the emulation board is directly connected to a host mainframe (as shown in Figure 2). Boyce ('258) does not expressly disclose the system comprising a debugger board including a debugger MCU for communicating with said debugger unit and with said target MCU, and for performing requests from said debugger unit and said target MCU, said debugger board further including a bus mapping unit, and a debugger RAM.

Autry ('695) teaches a system that uses a network adaptor to interface a debugging host with an emulator (see abstract). This adaptor necessarily includes a bus mapping unit (column 3 lines 25-28, the system converts network transmissions to emulator instructions) and RAM (column 8 lines 25-29, the communications manager performs fairly complicated protocol detection and selection algorithms).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the emulation system disclosed by Boyce ('258) such that it includes the network adaptor communication device, as disclosed by Autrey ('695) between the emulator board at the host mainframe. This modification would have been obvious because the use of physical connection hardware increases setup time (Autrey ('695)

column 2 lines 29-32) and limits the tester to a physical location near the system under test (Autry ('695) column 2 lines 35-38).

19. As per claims 11-18, these claims recite limitations found within claims 2-9, respectively. Claims 11-18 are rejected under Boyce ('258) in view of Autrey ('695) on the same grounds as cited with the respective 102(b) rejections of claims 2-9, above.

20. As per claim 19, this claim recites limitations found within claim 19, with the additional limitation of a the system comprising a debugger MCU, implemented with said target MCU, for communicating with said debugger unit and with said target MCU, and for performing request from said debugger unit and said target MCU.

In the system disclosed by Boyce ('258) a debug tool is used in conjunction with a mainframe computer with which a user performs debugging (column 1 lines 47-49). The mainframe translates a user's instructions into microprocessor-specific code (column 1 lines 49-52) and this requires a control unit.

21. As per claims 20-21, these claims recite limitations found within claims 2-3, respectively. Claims 20-21 are rejected under Boyce ('258) in view of Autrey ('695) on the same grounds as cited with the respective 102(b) rejections of claims 2-3, above.

22. As per claim 22, Boyce ('258) in view of Autrey ('695) discloses the apparatus of claim 19, further including a target/debugger board, connected to said debugger RAM board, that includes said target MCU and said debugger MCU.

23. Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyce ('258) in view of Winegarden (US Patent 6,691,266).

24. As per claim 26, Boyce ('258) discloses an apparatus for debugging an electronic system, said electronic system including a micro-controller ("target MCU") and at least one ROM connected together (column 2 lines 43-48), comprising:

a debugger unit for debugging said target MCU (column 1 lines 49-52);

a ROM/RAM emulator board, connected to said debugger unit (column 1 lines 49-52), said emulator board being disposed to emulate said ROM of said target MCU (column 1 lines 49-52), said emulator board including a ROM/RAM emulation memory and an emulator MCU (column 1 lines 57-61 and column 2 lines 43-48, while a microcontroller is not explicitly stated, it is required to perform the stated functions), said emulation memory being disposed to store user program codes downloaded from said debugger unit (column 2 lines 43-48), said emulator MCU being disposed to read and write data from and to said ROM/RAM emulation memory (column 2 lines 43-48); and

a target/debugger board, connected to said emulator board and to said debugger unit, said target/debugger board including said target MCU (column 1 lines 47-52, while

not physically connected, the mainframe is functionally connected to the target through the emulator).

Boyce ('258) does not explicitly disclose the system including a debugger MCU, implemented with said target MCU, for communicating with said debugger unit and said target MCU, and for performing requests from said debugger unit and said target MCU, said debugger MCU including an embedded RAM; and wherein the target/debugger board includes said debugger MCU and an embedded RAM.

Winegarden ('266) teaches an integrated circuit with an internal debugging unit that communicates with an external controller and an internal controller (the FPGA). The integrated circuit also contains memory (all as shown in figure 6).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the emulator system disclosed by Boyce ('258) such that the target chip includes an internal debugging unit that communicates with an external controller and an internal controller as shown by Winegarden ('266). This modification would have been obvious because the bus freezing causable by the debugger unit allows for increased hardware debugging flexibility (Winegarden ('266) column 6 lines 24-27).

25. As per claim 27, Boyce ('258) in view of Winegarden ('266) discloses the apparatus of claim 26, further comprising a debugger service routine ("debugger SR")

downloaded from said debugger unit into said ROM/RAM emulation memory with said user program codes from said debugger unit (Boyce ('258) column 1 lines 55-57).

26. As per claim 28, Boyce ('258) in view of Winegarden ('266) discloses the apparatus of claim 27, further comprising a communication buffer implemented in said emulation memory, said communication buffer being disposed to store status, request and data by said target MCU and by said debugger MCU (Boyce ('258) column 3 lines 49-54, execution results are returned to the debugger, and execution status is conveyed the execution results. Also see column 2 lines 45-47, command fragments of debug routines are passed through the communications buffer).

27. Claims 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyce ('258) in view of Gillenwater (US Patent Application Publication 2002/0053045).

28. As per claim 29, Boyce ('258) discloses an apparatus for debugging an electronic system, comprising:

a debugger unit (column 1 lines 49-52);

a ROM/RAM emulator/debugger/target board, connected to said debugger unit (column 1 lines 49-52), said emulator/debugger/target board including:

an emulator/debugger/target MCU having a target MCU that is debugged by the debugger unit (column 1 lines 57-61), the emulator/debugger/target MCU communicating with said debugger unit, and performing requests from said

debugger unit (column 2 lines 45-48) and said target MCU (column 2 lines 49-52, the end of routine message is the equivalent to a request for further routines or user action);

a bus mapping unit (column 2 line 67 through column 3 line 2);

a ROM/RAM emulation memory being disposed to store user program codes downloaded from said debugger unit (column 3 lines 10-13).

Boyce ('258) does not explicitly disclose the system including a target containing a debugger RAM and a ROM storing service routines.

Gillenwater ('045) teaches a controller containing basic debug routines in a ROM and updates or modifications to the debug routines in a complimentary RAM (paragraph 120).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the emulator system disclosed by Boyce ('258) such that the target unit includes a ROM storing service routines and a complimentary debugging RAM. This modification would have been obvious because the ROM allows for test routines to be stored on the device while the RAM allows for downloading test routine updates (Gillenwater ('045) paragraph 120).

29. As per claim 30, Boyce ('258) in view of Gillenwater ('045) discloses the apparatus of claim 29, further comprising a debugger service routine ("debugger SR") which is stored in the ROM memory (Gillenwater ('045) paragraph 120, the ROM is for debugging).

30. As per claim 31, Boyce ('258) in view of Gillenwater ('045) disclose the apparatus of claim 29, wherein said debugger RAM is implemented inside the emulator/debugger/target MCU (Gillenwater ('045) paragraph 120, a RAM is included with the device).

31. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boyce ('258) in view of Winegarden ('266) and Gillenwater ('045).

Boyce ('258) discloses an apparatus for debugging an electronic system, comprising:

a debugger unit (column 1 lines 49-52);

a ROM/RAM emulator/debugger/target board, connected to said debugger unit (column 1 lines 49-52), said emulator/debugger/target board including:

a ROM/RAM emulation memory being disposed to store user program codes downloaded from said debugger unit (column 3 lines 10-13).

Boyce ('258) does not explicitly disclose the emulator system wherein the emulator board includes a debugger MCU for performing requests from the debugger unit and target MCU, or where the emulator board includes a debugger RAM and a ROM.

Winegarden ('266) teaches an integrated circuit with an internal debugging unit that communicates with an external controller and an internal controller (the FPGA, as shown in Figure 6).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the emulator system disclosed by Boyce ('258) such that the target chip includes an internal debugging unit that communicates with an external controller and an internal controller as shown by Winegarden ('266). This modification would have been obvious because the bus freezing causable by the debugger unit allows for increased hardware debugging flexibility (Winegarden ('266) column 6 lines 24-27).

Gillenwater ('045) teaches a controller containing basic debug routines in a ROM and updates or modifications to the debug routines in a complimentary RAM (paragraph 120).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the emulator system disclosed by Boyce ('258) such that the target unit includes a ROM storing service routines and a complimentary debugging RAM. This

modification would have been obvious because the ROM allows for test routines to be stored on the device while the RAM allows for downloading test routine updates (Gillenwater ('045) paragraph 120).

Conclusion

The prior art made of record on accompanying PTO 892 form and not relied upon is considered pertinent to applicant's disclosure. Specifically, Zellmer ('364) teaches a memory mapper for an emulation circuit and Tung ('280) teaches a programmable emulator with a memory addressable target.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER